**Design of Low-Drop-Out Voltage Regulator in CMOS Technology for a Microprocessor Applications**

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**Abstract**

The demand for electronic devices has increased due to continues change in technology and its parameters. Low-Drop-Out [LDO] voltage regulator is used for power management and avoid unstable voltage used in many electronic applications. In this present investigation a comprehensive characterization of a low-dropout voltage regulator in Complementary metal oxide semi-conductor technology [CMOS] is simulated using mentor graphics tool. The error amplifier of the Linear dropout voltage employed 7 transistors for current mirror. By similar manner, the PMOS transistor is used as pass transistor to control the voltage difference. The resistors are used as a feedback network circuit while the capacitor is used to reduce the variation of output voltage. The results after execution shows that the proposed design provides a 1.6 V constant output voltage for the supply voltage ranges of 2 to 4.2 V. The dropout voltage of 140 mV is achieved with 1.6 mW power consumption.

**Keywords:** Current mirrors, Error amplifier, Mentor Graphics.

1. **Introduction**

The technology has been changing widely in electronic device where size and power decrease and frequency increases or operating speed of device increases due to these lot demand at electronic application. Recently, the rising demand for portable and battery-powered products has caused these circuits to run at low voltage conditions. To operate electronic device battery are use as voltage source. However, longtime is used of battery will lead to inactive voltage level. To keep away from inactive voltage level the Complementary metal oxide semiconductor linear voltage regulator will developed to control such problems. Where complementary metal oxide semi-conductor where it is a combination of P-MOS and N-MOS is used to design the digital circuit and it is a voltage-controlled device.

Low Drop-out voltage regulator are used at many electronic applications they required stable supply voltage provide by low dropout regulator it gives more current efficiency, less noise, more accuracy fast due to the lack of switching performance, proper power sources at a lower cost, and low standard current are all advantages. In addition, great current efficiency has It has become vital to maximize the battery's lifetime [1]. Battery is us as voltagee source, unstable voltage level occurs due to long period of battery use [2]. To avoid such problem CMOS Low drop out voltage regulator are used. LDO design has gotten more difficult as the demand for high-performance LDO’s has grown, with low-voltage fast-transient LDO, s being particularly significant [1]. it classified as low dropout, low supply current, high supply current, high-speed and high voltage [3]. The speed and power consumption are the two main factors for today portable applications [4]. For increased battery efficiency and longevity, low voltage and lower quiescent current are inherent circuit properties [5].

The working principle of low-drop-out voltage regulator is to provide accurate output voltage [6]. where output voltage while be stable by changing the input voltage and load impedance. It’s suitable for any equipment or electronic system that needs a constant output voltage, with improved supply voltage variations reduced and output voltage precision raised when some components are required. The advantages to use an LDO voltage

Low operating bias voltage, high efficiency performance, low power consumption, and high heat extraction are only a few of the benefits [7]. The LDO regulator was offered as a solo packaged device as well as an IP core that could be included into a larger integrated circuit design.

**2. Low Dropout Voltage Regulator**

The Low drop out voltage regulator consist of two feedback resistors, capacitors, error amplifier, reference source voltage and pass transistors [8]. The PMOS based LDO regulator is shown in Fig.1The power supply rejection is the main factor to determine the function of low dropout voltage regulator. In addition, the frequency compensation with power supply rejection enhancer is needed to improve the performance of power supply rejection and transient response in the low dropout voltage regulator circuit [8]. the dropout voltage, transient response, line regulation, efficiency, load regulation, power consumption, power supply rejection and quiescent current these all performances are improved by low dropout voltage regulator [9]. the power supply rejection ratio and transient response are main factors to determine the function of circuit these are raised by low drop out voltage regulator circuit [7]. Where power supply rejection ratio can be increased by frequency compensation with the power supply rejection enhance scheme the buffer is added between error amplifier and pass transistor to improve transient response [7-9].

**2.1. LDO Linear Regulator Architecture**

The basic structure of an LDO regulator typically includes a PMOS pass device, a decoupling capacitor CL with a parasitic resistor, two feedback resistors R1 and R2, and a reference resistor R2. Figure 1 shows a voltage and a critical error amplifier. There are three primary poles. p1 is from the output node, and p2 is from the input node. Comes from the pass device's gate, and p3 is the internal. Within the error amplifier, there is a pole [10]. A PMOS is used in the fundamental schematic of generic LDO voltage regulators. Between the input and output voltages, the PMOS FET with shared source connection acts as a pass transistor. R1 and R2 return a portion of the output voltage to the input, where it is compared to the voltage reference Vref and capacities load is represented by the capacitor CL [11].

The output of the regulator is the basis for LDO's operation yields an incorrect signal.to control the output current flow through a feedback network the transistor that allows information to pass through. The output voltage is maintained at a consistent level. R1, R2, and the reference voltage are used to determine the voltage level [12]. When the output voltage varies, the error amplifier is forced to adjust the current flow through PMOS due to divided voltage feedback through R1 and R2 and the reference voltage difference. To regulate the pass device, the error amplifier compares the error signal to the reference voltage and amplifies the difference. Controlling the load current flow through the pass device can result in a constant output voltage. Equation 1 determines the output voltage [12]. Equation (2) can be used to express the efficiency of an LDO regulator, while Equation (3) can be used to define the drop-out voltage (3)[12].

= x ----------- (1)

----------- (2)

= ---------- (3)

When the reference voltage and feedback voltage differ, an error signal is generated by the error amplifier. As shown in Figure 2, the error signal regulates the gate of the power transistor to maintain constant voltage with a variable current supply to the load circuit.

This topology has the benefit of a higher power supply rejection ratio (PSRR) and a dominant pole that is solely dictated by the load capacitance. To avoid decreasing the low voltage regulator (LVR) efficiency, the error amplifier's power consumption is kept to a minimum. It employs a centroid arrangement to reduce any voltage offset [13]. The pass element is used to raise the error amplifier's output current capabilities required by the load to higher levels in order to maintain a steady output value. It is necessary to transfer big currents from the source voltage to the load while the error amplifier's power regulation is low [7]. The pass element can be implemented using bipolar or MOS transistors. The MOS transistor has a lower power consumption and, as a result, a greater efficiency. The fundamental benefit of utilizing MOSFET as pass transistors is that, in addition to providing some gain, they are also self-protective against short circuit current. As a result, the extra short-circuit safety circuit is no longer required [14], N or P type MOS transistors are available. The power transistor, the NMOS, had a high dropout voltage. As a result, the gate voltage of the NMOS transistor must be greater than the source voltage. As a result, a charge pump is required to raise the voltage level [10].

PMOS LDO is the best solution for low voltage systems [14]. In order to produce a low dropout voltage, which also causes a stability issue [10]. The loop gain, bandwidth, stability, and dropout voltage are all influenced by the pass device. A sampling resistor in the feedback network reduces the output voltage to a reasonable level for comparison with the reference voltage by the error amplifier. Most transistors are intended to function in the sub threshold region to achieve low power and voltage operation with a tiny chip area, and no resistor or bipolar transistor is required in the voltage regulator. In general, a feedback network is a voltage divider that returns a portion of the regulated voltage to the error amplifier input. If the regulated voltage required is double that of the reference, The feedback network is made up of two identically resistive devices connected in series with one end to the output and the other to ground, with the centre point connected to the error amplifier. As a predetermined reference level, Vref is employed. The error amplifier compares a loaded feedback signal with Vref [15]. External capacitors off-chip are sometimes required by LDO regulators to improve transient responsiveness and stability [7]. Figure 3 depicts a voltage reference circuit [13].

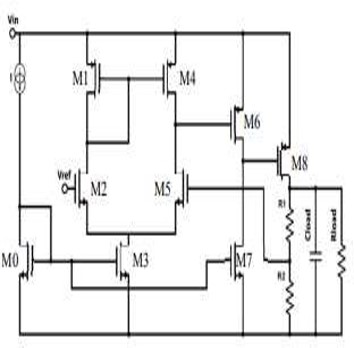


Figure 1: Schematic diagram of LDO

**2.2. Error Amplifier**

A negative feedback mechanism will be present in all power management ICs, which will use operational amplifiers to conduct the desired control actions. The control integrated circuits for adjustments to the power factor for the usage of error amplifiers the creation of the template required for moulding the input current which depicts the functional block diagram. Here an error amplifier is used [16] compares the output voltage to a reference, resulting in the error signal's needed magnitude. The error signal, which is a function of output voltage fluctuation, is multiplied by the sinusoidal current template to get the current template's magnitude. To create the requisite gate signals for the converter, the current template is compared to a ramp signal in an op-amp. It is evident from the receding explanation that operation amplifiers are critical components in any power management IC. The characteristics of op-amps such as DC gain, UGB, slew rate, PSRR, and CMRR determine the controller's capacity to shape the input current in the form of a sine function. Commercial error amplifiers are not optimised, and design requirements are frequently proprietary in nature. The current research goal is to create a power factor controller with all of the essential control functions. Guidelines are provided in this publication [17].

A DC connected high gain electronic voltage amplifier with a differential input and a single-ended output is known as an operational amplifier (Op amp). They're used in anything from dc bias to high-speed amplifiers and filters. Generally, Op amps can be used for a variety of purposes, including buffers, summers, integrators, differentiators, comparators, negative impedance converters, and more. It is proposed to develop an error amplifier with the desired parameters.

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Op-amps (error amplifiers), on the other hand, utilise negative feedback designs that must be corrected in order to produce high gain and excellent phase margins with a higher cross over frequency. In order to create an op amp, the analogue circuit designer must go through various procedures or phases [19]. The designer evaluates the Op amp's intended use, determines performance parameters, and chooses a suitable circuit architecture in the first step. The topology is scaled and biased using analytical first order design equations in the second step. The design is assessed and optimised in the third step by adjusting design parameters and repeating circuit simulation [20].

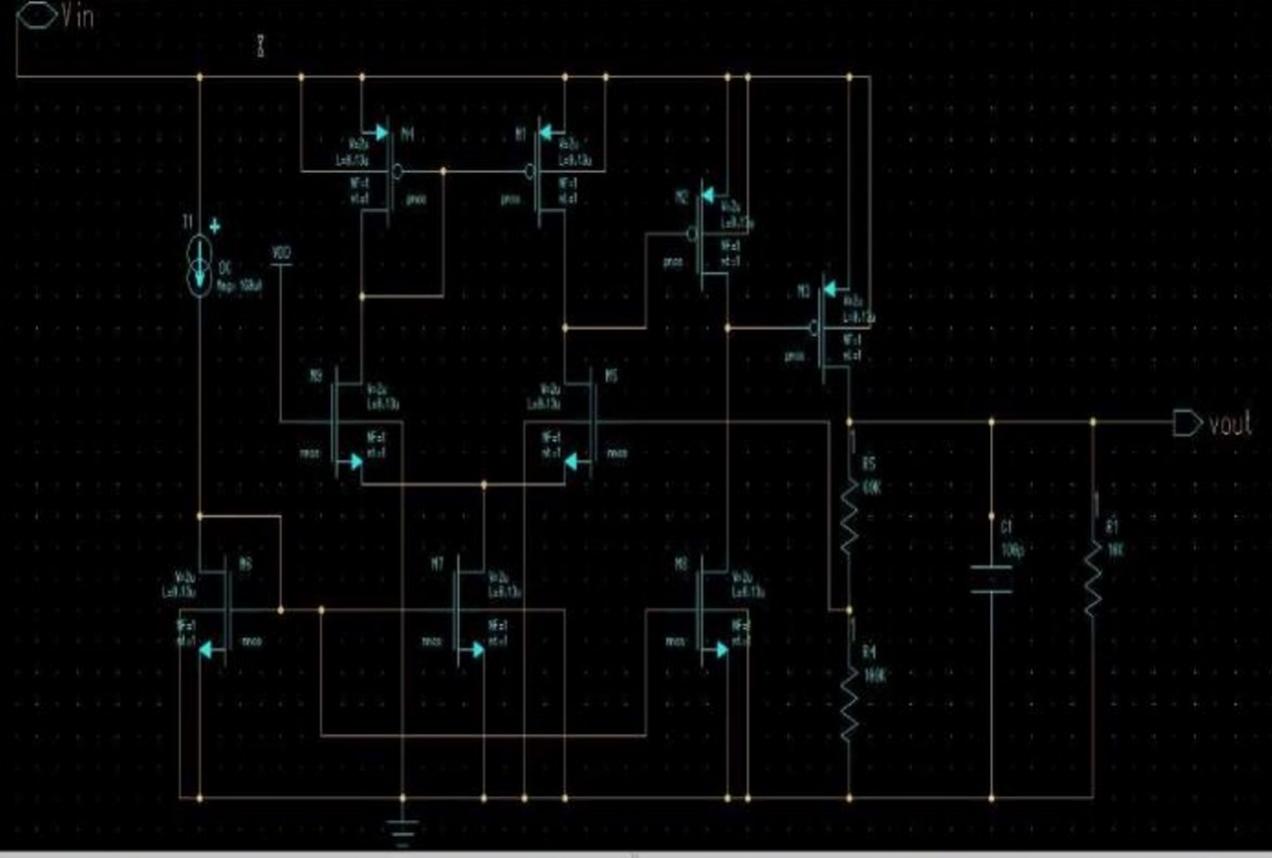


Figure 2: Circuit design of resistance values are R1 = 60 KΩ and R2=100 KΩ.

**3. Fundamental Evaluation and Discussion**

The output voltage of the linear voltage output from 2.4 V is dependent on the feedback resistors R1 and R2, which have values of 60 kΩ and 100 kΩ respectively. Where the production is influenced by the Vout = Vref (1 + R1/R2), Vref and feedback resistance play a role. To obtain in order to achieve linear voltage regulation, an error amplifier is used with feedback resistors. It was used to control the input voltage using a voltage reference, and the output voltage of the resistor is constant, yielding a voltage of 2.4 V.

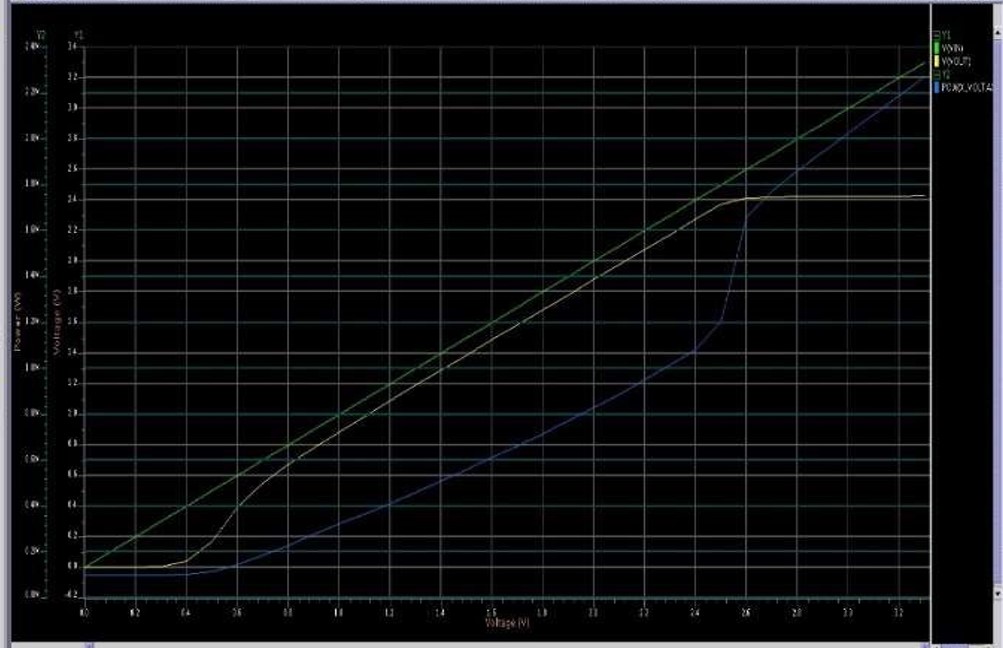


Figure 3: Simulated Output voltage vs input voltage of LDO Regulator

The linear voltage regulation of 1.6 V from 2 to 4 V input supply voltage is depicted in figure (2). The output voltage is influenced by the feedback resistors R1 and R2, which have values of 6 kΩ and 10 kΩ, respectively. In feedback unidirectional voltage control circuits, we used an error amplifier to achieve linear voltage regulation by sampling the output voltage of the circuit under control and comparing it to a stable reference value. Before that unstable output voltage and after that steady voltage, receive the output of 1.6 V and the input voltage from 2 to 4 V.

The output voltage and PSRR (power supply rejection ratio) for 60 kΩ and 100 kΩ resistors were computed using mentor graphics Programme and CMOS technology, where yellow line is the output and blue PSRR is the output for 60 kΩ and 100 kΩ resistors is 2.4 V linear voltage and PSRR is 1.6 mV.

**4. Conclusion**

We use mentor graphic software to develop a low-drop power regulator in CMOS technology that uses an error amplifier as an input voltage controller and provides a constant output based on a feedback resistor linked MOS transistors, resistors, and capacitors are used where MOS transistors are employed. Transistors and resistors are utilized to regulate the leakage current. The capacitor serves as a voltage divider that operates on a reference voltage. Where the input voltages Vin and Vref vary from 2.55 to 3.55 V in which the output is a constant voltage linear voltage of 2.41 V The feedback resistance values are 6 kΩ and 10 kΩ, respectively, while the load resistance is 10 kΩ, 1.5 volts is the reference voltage. The linear drop out voltage regulator will be employed in a variety of applications such as mobile phones, iPods, tablets, and microprocessors.

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